Efficient Computing System for Satellite Image Processing Processor

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Approximate computing plays a significant role in signal processing and image processing applications. Radix-8 approximate novel booth multiplier (R8ANBM) based on approximate novel booth encoder (ANBE) is proposed in this paper to validate approximate computing. The proposed design is synthesized and simulated in Xilinx ISE 13.2. The experimental results show that the proposed multiplier performs better in terms area, speed and energy consumption. The proposed R8ANBE reduced the number of 4 input LUTs by 23.07%, 17.94%, 19.87%, 16.66%, 13.46%, 8.33%, 12.82%, 9.61%, 12.17% and number of occupied slices by 22.33%, 30.09%, 25.24%, 29.12%, 14.56%, 17.47%, 13.59%, 12.62%, 17.47% when compared with the existing techniques such as conventional booth multiplier, R4ABM1, RAD64, ABM1, HLR-BM1, HLR-BM2, R8ABM1, R8ABM2, R8ABM3 respectively. It achieved the accuracy as 67.3% which is higher than exisitng approximate booth multipliers. The proposed R8ANBM is applied to image sharpening applications and the performances are analyzed in terms of error metrics such as ralative mean error distance, normalized mean error distance and peak signal to noise ratio. The above proposed system was implemented using 45nanometer technology library. With applications in low-power CMOS design, quantum computing, optical information processing, DNA computing, bioinformatics, and nanotechnology, there is an increasing interest in power minimization.

Povzetek: Predstavljena je izboljšana pomnilniško učinkovita porazdeljena arhitektura za 2D diskretno valčno transformacijo (DWT), prilagojeno satelitskim slikam. Z uporabo stiskanja iskalne tabele (LUT) predlagana zasnova zmanjšuje pomnilniške zahteve, hkrati pa ohranja računsko učinkovitost, kar predstavlja pomemben prispevek k visoko zmogljivim VLSI implementacijam za obdelavo slik.

1 Introduction

In this modern world, one of the recent trends in VLSI design is approximate computing which focused the tradeoff factors area, power consumption and speed. In this emerging computing method, the internal structure of the architecture is modified by eliminating certain logic gates which leads to the erroneous output for some cases. But this error is acceptable in image processing applications, data mining, filtering, digital signal processing, machine learning, computer vision, etc [1]. Due to the advantages of approximate computing [2], the researchers concentrate on different approximation approaches and utilize these approaches in certain applications. In addition to that, approximate computing plays a significant role in hardware accelerators for customization of the hardware modules and for processing large amount of data [3].

Approximate accelerators are designed in [4] by collecting the most appropriate approximate elements from libraries where lot of approximate arithmetic circuits are stored. It uses space exploration methodology for approximate circuit collection and uses machine learning techniques for estimation of computational modules. The fundamental components involved in the approximate accelerator are approximate adder and approximate multiplier. So these should be designed with low power consumption and high performance to make it well suited for effective applications. Approximate computing is also applicable for biometric security systems [5]. In this method, the runtime of the application is reduced by applying the encoding techniques to the resultant obtained from iris scanning.

Multiplier is a power-hungry arithmetic circuit used in most of the signal processing applications. To reduce the power consumption of the multiplier designs, approximate multipliers are focused by the researchers [6]. In approximate multiplication, the approximation is inserted in partial product formation or partial product reduction or partial product summation. Most of the approximation approaches uses encoding process for the partial products to reduce the complexity of the design. Then the encoded partial products are compressed with the help of approximate half adder and approximate full adder [7].

This paper proposed an approximate novel booth encoder (ANBE) for radix-8 booth multiplication. The proposed encoder reduces the number of partial products leads to the reduction in the complexity. It uses approximate half adders to generate the 3X product term thereby it facilitates the simplest method to partial product formation. The proposed radix-8 booth multiplier using ANBE is designed in Xilinx ISE 13.2 and coded in

Verilog HDL. The proposed radix-8 approximate novel booth multiplier (R8ANBM) outperforms better than existing radix-8 booth multipliers. At long last, the fruitfulness of the proposed radix-8 booth multiplier design is demonstrated with image sharpening applications.

The remaining section of this research work is as follows. Section 2 describes the works related with booth encoders and approximate multipliers. Section 3 presents the proposed approximate novel booth encoder. It also explains the logical diagram and operation of the ANBE. Section 4 explains the proposed radix-8 approximate booth multiplier and Image sharpening using proposed booth multiplier. Performance analysis is given in Section 5 and error analysis is given in Section 6. Finally, the work is concluded in Section 7.

2 Related work

Multipliers have significant importance in image processing and signal processing applications. Honglan Jiang presented an approximate radix-8 booth multiplier based on encoding methods which is used for reducing the partial product count [8]. This approximate multiplier eliminates the complexity of conventional radix-8 booth multiplier by the exploitation approximate adder which computes the sum of 1X and 2X products. This multiplier is applied in the filtering applications to evaluate the performance of the approximate radix-8 booth multiplier. The observation results showed that, there is a tradeoff between power consumption and accuracy.

Area and power efficient booth multiplier are designed in [9]. The adder and subtractor used in this multiplier are designed using multiplexers. The code block also fully designed by multiplexers. In this booth multiplier, there are no components other than multiplexers and it is well suited for graphics applications. V. Leon et al presented hybrid radix encoding techniques for partial product formation. This hybrid approach is suitable for signed multiplier where approximate radix-4 encoding approach is used in least significant bits and accurate approach is used in most significant bits [10]. In this method the highest radix values are converted to two the power of values and it is termed as rounding. Since it achieves high energy efficiency, there is a tradeoff between energy consumption and accuracy.

8 point Fast Fourier Transform is designed using approximate radix-8 booth multiplier [11] which partially performed the operation of butterfly unit. The remaining operation of butterfly unit is performed by recoded adder and Kogge Stone adder. It utilized the approximation approaches for generating 3X product leads to low power consumption. It also uses external circuit for error detection as well as error correction leads to more area. Suganthi Venkatachalam designed three different approximate booth multipliers ABM1, ABM2 and ABM3 [12]. Here, the approximation is inserted in the booth encoding process. It reduces the logic complexity presents in the partial product formation. This design is applied in Finite Impulse Response (FIR) filter to evaluate the performance of ABM1, ABM2 and ABM3. These are performing better in terms of area and power consumption with delay overhead.

Alberto A. Del Barrio et al designed a carry save radix-8 booth multiplier [13] that reduced the number of partial product rows into half. It uses 4:2 compressors for forming partial product matrix (PPM) and Kogge Stone adder for carry propagate addition. It increased the speed with area overhead due to the utilization of parallel prefix adder. Bayadir A. Issa et al designed a fused multiply add unit using radix-8 booth multiplier. It is represented in floating point format and so the 53x53 bit mantissa product is obtained by performing booth multiplication [14]. The partial products are reduced with the aid of 4:2 carry save adder tree which increased the speed of the whole unit. Jiang et al [15, 16] compared approximate arithmetic circuits to utilize these in the accumulation stages. High accuracy fixed width booth multipliers are designed and its error metrics are analyzed in [17, 18]. Choi et al [19] designed hybrid radix truncated multiplier for mobile applications. Different booth encoding approaches, approximation techniques, booth multiplier structures are discussed [20-23] to evaluate the limitations of these approaches.

3 Proposed approximate novel booth encoder (anbe)

Let A is n-bit signed multiplicand and B is n-bit signed multiplier and these are expressed in two's complement format.

$$A = -a_{n-1}2^{n-1} + \sum_{p=0}^{n-2} a_p 2^p \quad (1)$$

$$B = -b_{n-1}2^{n-1} + \sum_{p=0}^{n-2} b_p 2^p \quad (2)$$

The product can be obtained by applying novel booth encoding approach to the multiplicand B.

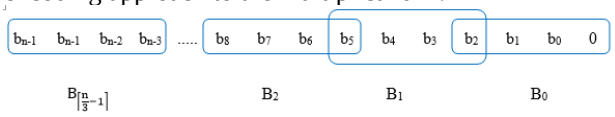

Figure 1: Grouping of multiplier bits for booth encoding

Every four bits are grouped from right to left and it is termed as a set {b_(3q+2), b_(3q+1), b_3q, b_(3q-1)}. During this group formation, the least significant bit (b_ (-1)) is assigned as zero and the most significant bit (b_(n-1)) is assigned as sign bit. Before encoding process, the multiplier bits are grouped into various sets and it is depicted in Figure 1. The encoded format for every group is represented by the following equation

$$B_q = -4b_{3q+2} + 2b_{3q+1} + b_{3q} + b_{3q-1} \quad (3)$$

In equation (1), the value of m should be lies between 0≤ q ≤(⌈n/3⌉-1). Here, the value of B_q may be 0, -1, -2, -3, -4, +1, +2, +3 or +4. Every group of

multipliers is multiplied with the multiplicand to get the partial products and it can be represented as follows.

$$Ppq=A*B\_q \quad (4)$$

where Ppq represents partial products in the mth row. For every group, the most significant bit of the encoded values is considered for sign computation. If it is zero, it is termed as positive, otherwise termed as negative. During the positive cases, 2 x multiplicand (2A) can be obtained by left shifting the A by one bit and 4 x multiplicand (4A) can be obtained by left shifting the A by two bits. 3 x multiplicand (3A) can be obtained by adding A and 2A. When the sign is negative, then two's complement is applied to get the partial product row. The logic diagram of existing R8ABE1 is shown in Figure 2.

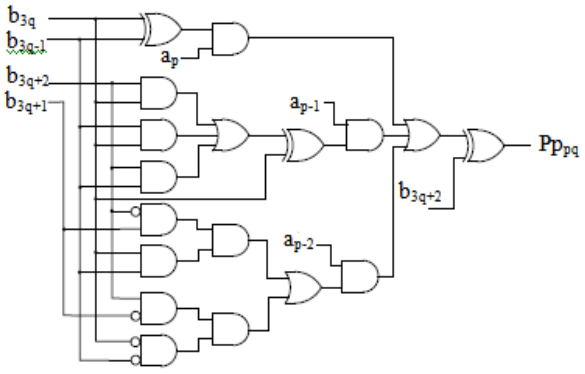

Figure 2: Logic diagram of existing R8ABE1

In R8ABE1, the partial product Pppq can be computed by the following expression.

$$Pp_{pq} = \left[a_p(b_{3q} \oplus b_{3q-1}) + a_{p-1}\left(b_{3q} \oplus (b_{3q+2}b_{3q} + b_{3q-1}b_{3q} + b_{3q+2}b_{3q-1})\right) + a_{p-2}(\bar{b}_{3q+2}b_{3q+1}b_{3q}b_{3q-1} + b_{3q+2}\bar{b}_{3q+1}\bar{b}_{3q}\bar{b}_{3q-1})\right] \oplus b_{3q+2} \quad (5)$$

The logic equation of the existing R8ABE1 is modified to reduce the area as well as power consumption of the encoder design. The logic expression given in (5) is simplified to get the novel approximate booth encoder. The partial product bit Pppq at qth row in pth position can be expressed by the following equation

$$Pp_{pq} = [a_p(b_{3q} \oplus b_{3q-1}) + (a_{p-1}(\bar{b}_{3q-1}b_{3q}\bar{b}_{3q+2} + b_{3q-1}\bar{b}_{3q}b_{3q+2}) + a_{p-2}(b_{3q-1}b_{3q}b_{3q+1}\bar{b}_{3q+2} + \bar{b}_{3q-1}\bar{b}_{3q}\bar{b}_{3q+1}b_{3q+2})] \oplus b_{3q+2} \quad (6)$$

The logic diagram of the proposed ANBE is shown in Figure 3. The proposed approximate novel booth encoder reduces the area by reducing the number of logic gates. It requires 31 logic gates to complete the encoder design which is lesser than existing R8ABE1 that requires 35 logic gates. So, 4 logic gates are reduced for every partial product row. If there is y number of partial product rows, then 4y logic gates are reduced.

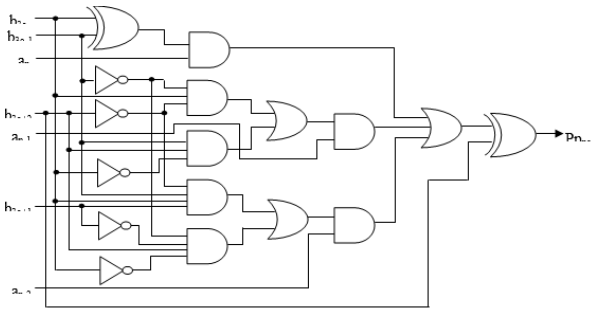

Figure 3: Logic diagram of the proposed ANBE

The truth table of the proposed ANBE is tabulated in Table 1.

Table 1: Truth table of the proposed ANBE

b_{3q+2}	b_{3q+1}	b_{3q}	b_{3q-1}	B_q	Pp_{pq}
0	0	0	0	0	0
0	0	0	1	1	a_p
0	0	1	0	1	a_p
0	0	1	1	2	a_{p-1}
0	1	0	0	2	a_{p-1}
0	1	0	1	3	$a_p + a_{p-1}$
0	1	1	0	3	$a_p + a_{p-1}$
0	1	1	1	4	a_{p-2}
1	0	0	0	-4	$\bar{a}_{p-2}$
1	0	0	1	-3	$\overline{a_p + a_{p-1}}$
1	0	1	0	-3	$\overline{a_p + a_{p-1}}$
1	0	1	1	-2	$\overline{a_{p-1}}$
1	1	0	0	-2	$\overline{a_{p-1}}$
1	1	0	1	-1	$\bar{a}_p$
1	1	1	0	-1	$\bar{a}_p$
1	1	1	1	0	0

From Table 1, it is observed that, the proposed ANBE cannot generate the exact output in 4 cases. 〖Pp〗_pq generate erroneous outputs when B_q=+3 and B_q=-3. In four cases, B_q=±3 is present; hence the probability of error is 4/16 as ¼

4 Proposed radix-8 anbe based multiplier (r8anbm)

Three major operations of multiplier are partial product generation, reduction and addition. The additional process involved in the booth multiplier is booth encoding. Since this research focused the approximate booth multiplier, approximate booth encoder is proposed. In this proposed multiplier, the partial products are generated by approximate novel booth encoding approach. The positioning of these partial products is same as the existing booth multiplier. Then the reduction of partial products is performed by 4:2 compressors, full adder and half adder. Finally, the reduced partial products are added with the area efficient and high-speed Brent Kung (BK) adder.

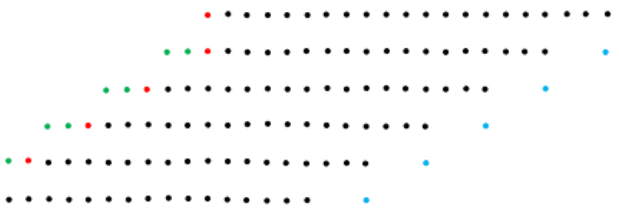

Figure 4: Dot diagram of proposed Radix-8 approximate novel booth multiplier

The dot diagram of proposed radix-8 approximate novel booth multiplier is shown in Figure 4. The blue colour, red colour and green colour denotes the sign of booth encoded digits, inverted sign bit and binary one respectively. After forming these encoded products, the partial products are accumulated using compressors and finally these are added using two operand adders.

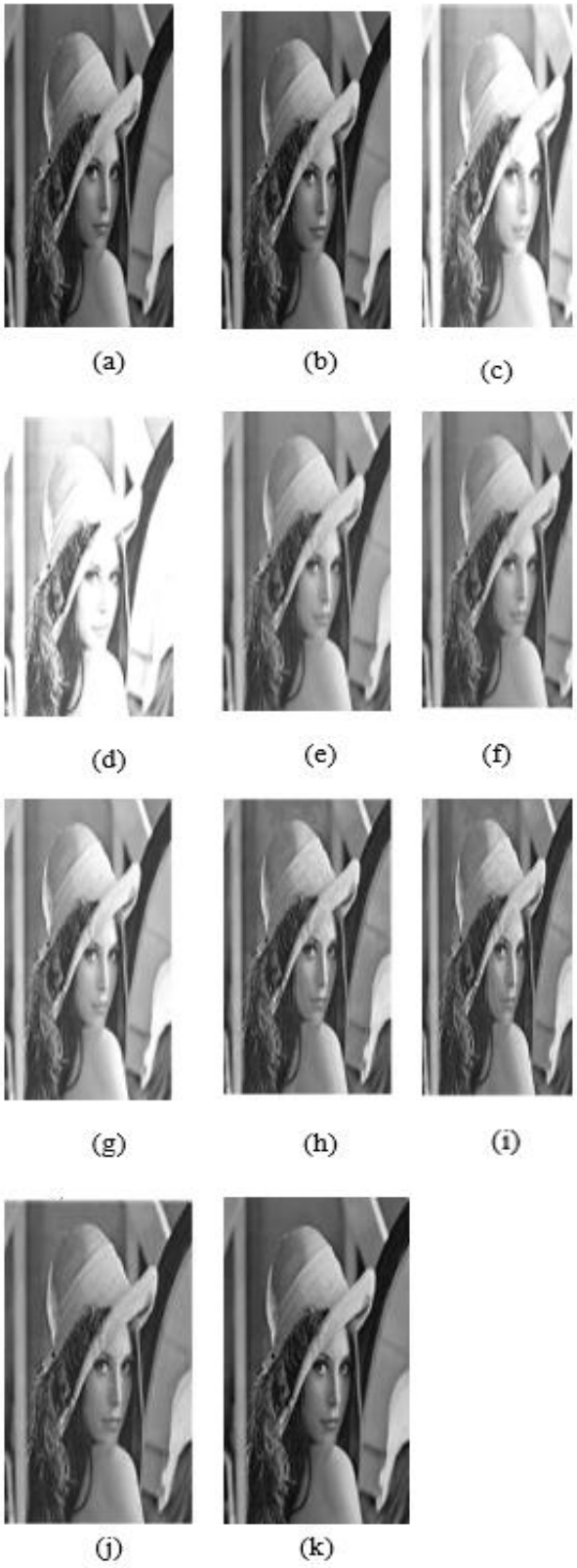

Figure 5: Image sharpening with different approximate booth multipliers: (a) Input Image, (b) Conventional booth multiplier, (c) R4ABM1, (d) RAD64, (e) ABM1, (f) HLR-BM1, (g) HLR-BM2, (h) R8ABM1, (i) R8ABM2, (j) R8ABM3, (k) Proposed R8ANBM

The 225x225 grey scale image is selected for quality evaluation. Image compression using different approximate booth multipliers are analyzed and output images are shown in Figure 2.

5 Performance analysis

The proposed R8ANBM multiplier and the existing multipliers are designed and simulated using Xilinx ISE 13.2 and these are coded using Verilog HDL. The performances of the proposed R8ANBM are analyzed in terms of area, delay and energy efficiency.

Table 2: Gate count of booth encoders

Technique	Number of logic gates
Conventional booth encoding	38
R8ABE1	35
R8ABE2	34
R8ABE3	35
R8ANBE	31

Area is analyzed in terms of number of 4 input LUTs, occupied slices and number of logic gates. Area of the proposed ANBE is compared with the existing booth encoding approaches and it is tabulated in Table 2. From Table 2, it is cleared that the proposed ANBE requires a smaller number of logic gates which is lesser than other existing approaches. R8ANBE has 22.58%, 12.90%, 9.67% and 12.90% less gate count than conventional booth encoding, R8ABE1, R8ABE2 and R8ABE3 respectively.

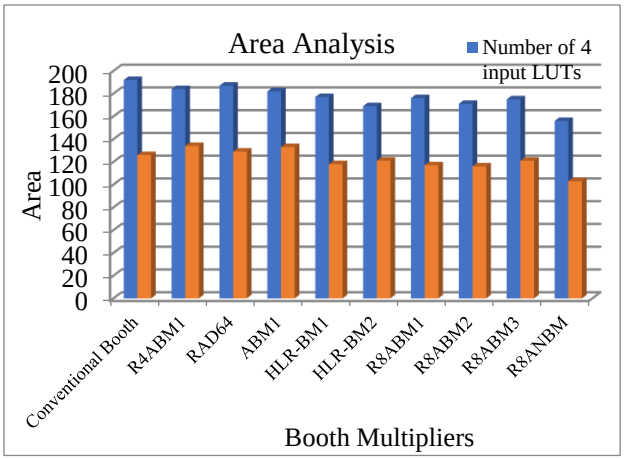

Figure 6: Area analysis of approximate booth multipliers

Area of the proposed radix-8 approximate multiplier using novel booth encoder is compared with the existing booth multipliers and it is shown in Figure 3. From the comparison chart, it is observed that, the proposed ANBE reduced the area over ther existing multiplier designs. The proposed R8ANBE reduced the number of 4 input LUTs by 23.07%, 17.94%, 19.87%, 16.66%, 13.46%, 8.33%, 12.82%, 9.61%, 12.17% and number of occupied slices by 22.33%, 30.09%, 25.24%, 29.12%, 14.56%, 17.47%, 13.59%, 12.62%, 17.47% when compared with the existing techniques such as conventional booth multiplier, R4ABM1, RAD64, ABM1, HLR-BM1, HLR-BM2, R8ABM1, R8ABM2, R8ABM3 respectively.

Time consumed by the different approximate multipliers to complete the operation is expressed in the comparison chart and it is shown in Figure 4. The proposed R8ANBM has reduced the delay by 31.86%, 29.24%, 27.91%, 30.94%, 27.51%, 24.87%, 16.03%, 18.45% and 18.88% when compared with the existing techniques such as conventional booth multiplier, R4ABM1, RAD64, ABM1, HLR-BM1, HLR-BM2, R8ABM1, R8ABM2 and R8ABM3 respectively.

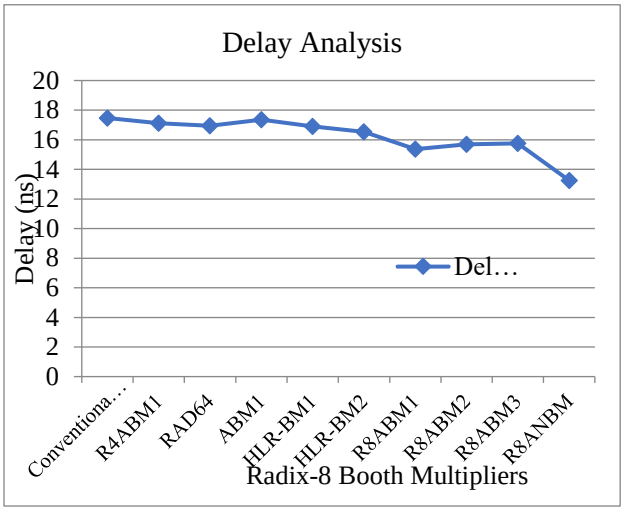

Figure 7: Delay analysis of approximate booth multipliers

Energy consumption of the approximate multiplier design is the power delay product. Energy consumption of various approximate booth multipliers are compared and it is tabulated in Table 3.

Table 3: Energy consumption comparison of approximate booth multipliers

Technique	Energy Consumption (nJ)
Conventional Booth	4.917
R4ABM1 [20]	4.521
RAD64 [21]	3.895
ABM1 [22]	3.567
HLR-BM1 [3]	3.125
HLR-BM2 [3]	2.992

R8ABM1 [23]	2.736
R8ABM2 [23]	2.557
R8ABM3 [23]	2.667
Proposed R8ANBM	2.132

From the tabulated results, it is observed that the proposed R8ANBM reduces the energy consumption by 56.64%, 52.84%, 45.26%, 40.22%, 31.77%, 28.74%, 22.07%, 16.62% and 20.05% when compared with conventional booth multiplier, R4ABM1, RAD64, ABM1, HLR-BM1, HLR-BM2, R8ABM1, R8ABM2 and R8ABM3. The proposed R8ANBM performs better in terms of area, speed and energy consumption.

6 Error analysis

The error fed by the approximate novel booth encoder in the proposed approximate novel booth multiplier is analyzed in terms of normalized mean error distance (NMED), mean relative error distance (MRED), accuracy and peak signal to noise ratio (PSNR). These error metrics are based on error distance which can be computed by calculating the difference between exact product and inexact product. MED is defined as the average values of error distance for all possible input combimations. NMED is the normalization of MED values [24] and it can be computed by the following expression.

$$NMED = \frac{1}{2^{2n}} \sum_{p=1}^{2^{2n}} \left| \frac{ED_p}{\max ED} \right| \quad (6)$$

Here, n denotes the bit width of multiplicand and multiplier. EDp denotes the error distance value of pth input combination. Max ED denotes maximum error distance value of the outputs. MRED is defined as the mean value of the ratio of error distance to the exact output for all possible combination of inputs. It can be computed by the following expression.

$$MRED = \frac{1}{2^{2n}} \sum_{p=1}^{2^{2n}} \left| \frac{ED_p}{EO_p} \right| \quad (7)$$

Here, EO denotes the exact output at pth combination of input. The accuracy of the proposed R8ANMB is the ratio of number of exact outputs to the total number of outputs and it can be expressed as follows.

$$Accuracy\ (\%) = \frac{Number\ of\ exact\ outputs}{Total\ number\ of\ outputs} \times 100 \quad (8)$$

The accuracy of the design is directly proportional to the number of exact outputs. So, the accuracy is improved by increasing the number of exact outputs.

Table 4: Error analysis of approximate radix-8 booth multipliers

Technique	NMED (x10-3)	MRED (x10-2)	PRED	Accuracy (%)
Conventional Booth	0	0	100	100
R4ABM1	8.425	3.478	98.51	45.38
RAD64	4.790	4.001	99.58	41.12
ABM1	5.472	1.276	99.68	44.98
HLR-BM1	7.914	3.045	98.35	64.89
HLR-BM2	6.185	2.151	99.12	63.24
R8ABM1	5.221	1.221	99.54	55.26
R8ABM2	6.245	2.027	99.01	42.71
R8ABM3	8.174	1.764	99.41	59.54
R8ANBM	3.114	0.923	99.76	67.15

Error metrics in terms of NMED, MRED and accuracy of the proposed R8ANBM are compared with the existing approximation booth multipliers and it is tabulated in Table 4. The tabulated results showed that the proposed R8ANBM reduces the NMED by 63.03%, 34.98%, 43.09%, 60.65%, 49.65%, 40.35%, 50.13%, 61.90% and MRED by 73.46%, 76.93%, 27.66%, 69.68%, 57.08%, 24.40%, 54.46%, 47.64% when compared with R4ABM1, RAD64, ABM1, HLR-BM1, HLR-BM2, R8ABM1, R8ABM2, R8ABM3 respectively. The proposed R8ANBM achieves better accuracy than exisiting approximate booth multipliers. The conventional accurate booth multiplier achieves 100% accuracy. The proposed R8ANBM achieved the accuracy as 67.15% which was increased by 32.41%, 38.76%, 33.01%, 3.36%, 5.82%, 17.70%, 36.39% and 11.33% when compared with R4ABM1, RAD64, ABM1, HLR-BM1, HLR-BM2, R8ABM1, R8ABM2 and R8ABM3 respectively.

In image sharpening applications, PSNR is one of the error metrics used to evaluate the quality of the output images. PSNR is measured in decibel and it can be computed by the following expression

$$PSNR = 10log_{10}\left(\frac{max_p^2}{MSE}\right) \quad (9)$$

where, max p denotes the input image's maximum pixel value and MSE denotes mean square error value of the image.

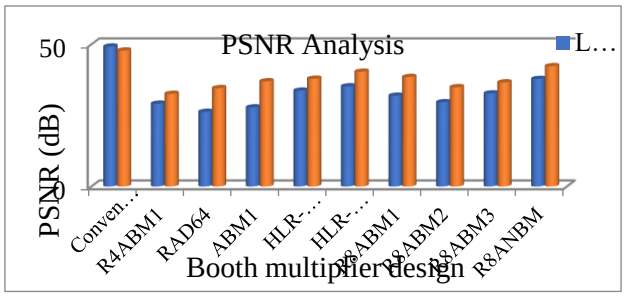

Figure 8: PSNR comparison of booth multipliers with two different test images

Image sharpening of radix 8 booth multipliers is tested with two different test iamges (Lena and Barbara) and its PSNR values are computed to show the effectivity of the proposed R8ANBM multiplier. From Figure 5, it is exhibited that, the proposed R8ANBM multiplier has low PSNR values compared with conventional booth multiplier and high PSNR values compared with another existing approximate booth multiplier. The proposed R8ANBM has 18.49%, 27.70%, 15.59% high PSNR for lena image and 9.87%, 21.20%, 15.57% high PSNR for barbara image compared to the existing approximate booth multipliers such as R8ABM1, R8ABM2, R8ABM3 respectively.

7 Conclusion

This paper talk about the approximate novel booth encoder design and radix-8 approximates novel booth multiplier based on ANBE. The accuracy of the proposed R8ANBM is high over other approximate booth multipliers, due to the less error probability of ANBE. Less number logic gates requirement in ANBE design leads to low area and low energy consumption in multiplier design. It also performs better in terms of NMER and MRED. The proposed R8ANBM reduces the NMED by 63.03%, 34.98%, 43.09%, 60.65%, 49.65%, 40.35%, 50.13%, 61.90% and MRED by 73.46%, 76.93%, 27.66%, 69.68%, 57.08%, 24.40%, 54.46%, 47.64% when compared with R4ABM1, RAD64, ABM1, HLR-BM1, HLR-BM2, R8ABM1, R8ABM2, R8ABM3 respectively. The proposed R8ANBM is analyzed for image sharpening applications. It can achieve high PSNR value as 37.8 for lena image and 42.3 for barbara image. The proposed R8ANBM achieved the accuracy as 67.15% which was increased by 32.41%, 38.76%, 33.01%, 3.36%, 5.82%, 17.70%, 36.39% and 11.33% when compared with R4ABM1, RAD64, ABM1, HLR-BM1, HLR-BM2, R8ABM1, R8ABM2 and R8ABM3 respectively. The proposed system is suitable for nanotechnology applications to reduce the power effectively.

Author contributions statement

"A. Azhagu Jaisudhan Pazhani done implementation of algorithms, methodology, preparation of flow chart and manuscript, result analysis for the manuscripts."

Conflict of interest

There is no conflict of interest in this paper regarding publication.

Data availability statement

The data that supports the findings of this study are available within the article.

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References

[1] B. Liu, Z. Wang, S. Guo, H. Yu, Y. Gong, J. Yang, L. Shi (2019), 'An energy efficient voice activity detector using deep neural networks and approximate computing', in Microelectronics Journal, vol. 87, pp. 12-21.

[2] S. Xu, and B. C. Schafer (2019), 'Toward Self-Tunable Approximate Computing', IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 27, no. 4, pp. 778-789.

[3] Haroon Waris, Chenghua Wang, and Weiqiang Liu (2020), 'Hybrid Low Radix Encoding based Approximate Booth Multipliers', vol. 67, no. 12, pp. 3367-3371.

[4] V. Mrazek, M. A. Hanif, Z. Vasicek, L. Sekanina, and M. Shaffique (2018), 'autoAx: An Automatic Design Space Exploration and Circuit Building Methodology utilizing Libraries of Approximate Components', in Proceedings of the 56th Annual Design Automation Conference (DAC), Las Vegas, pp 588-601.

[5] Soheil Hashemi, Hokchhay Tann, Francesco Buttafuoco, Sherief Reda (2018), 'Approximate Computing for Biometric Security Systems: A Case Study on Iris Scanning', Design, Automation & Test in Europe Conference & Exhibition (DATE).

[6] Paladugu Srinivas Teja (2014), 'Design of Radix-8 Booth Multiplier Using Koggestone Adder for High-Speed Arithmetic Applications', Emerging Trends in Electrical, Electronics & Instrumentation Engineering: An international Journal (EEIEJ), vol. 1, no. 1, pp. 45-55.

[7] Nimmy Joseph, David Solomon George and K. Sajitha (2020), 'Power efficient approximate multiplier with reduced complexity using encoded partial products', AIP Conference Proceedings, pp. 020007(1-6).

[8] Honglan Jiang, Jie Han, Fei Qiao, and Fabrizio Lombardi (2016), 'Approximate Radix-8 Booth Multipliers for Low-Power and High-Performance

Operation', IEEE Transactions on Computers, vol. 65, no. 8, pp. 2638 – 2644.

[9] V Soma Sandeep, K Bala Sindhuri, N Udaya Kumar and K Rajesh (2018), 'Design of Area and Power Potent Booth Multiplier Using Multiplexer', Proceedings of the International Conference on Communication and Electronics Systems (ICCES), pp. 1-6.

[10] V. Leon, G. Zervakis, D. Soudris and K. Pekmestzi (2018), 'Approximate Hybrid High Radix Encoding for Energy-Efficient Inexact Multipliers', IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 26, no. 3, pp. 421-430.

[11] Anil Kumar Reddy Y and Sathish Kumar P (2018), 'Performance Analysis of 8-Point FFT using Approximate Radix-8 Booth Multiplier', Proceedings of the International Conference on Communication and Electronics Systems (ICCES), pp. 42-45.

[12] S. Venkatachalam, E. Adams, H. J. Lee and S. Ko (2019), 'Design and Analysis of Area and Power Efficient Approximate Booth Multipliers', IEEE Transactions on Computers, vol. 68, no. 11, pp. 1697-1703.

[13] Alberto A. Del Barrio, Román Hermida, and Seda Ogrenci-Memik (2019), 'A Combined Arithmetic-High-Level Synthesis Solution to Deploy Partial Carry-Save Radix-8 Booth Multipliers in Datapaths', IEEE Transactions on Circuits and Systems–I: Regular Papers, vol. 66, no. 2, pp. 742-755.

[14] Bayadir A. Issa, Israa Sabri A. AL-Forati, Mohammed A. Al-Ibadi, Hayder M. Amer, Abdulmuttalib Turky Rashid and Osama T. Rashid (2020), 'Design of High Precision Radix-8 MAF Unit with Reduced Latency', International Congress on Human-Computer Interaction, Optimization and Robotic Applications (HORA), pp. 1-7.

[15] H. Jiang, C. Liu, L. Liu, F. Lombardi, and J. Han (2017), 'A review, classification, and comparative evaluation of approximate arithmetic circuits', ACM Journal on Emerging Technologies in Computing Systems (JETC), vol. 13, no. 4, pp. 1-34.

[16] V. Leon and K. Asimakopoulos and S. Xydis and D. Soudris and K. Pekmestzi (2019), 'Cooperative Arithmetic-Aware Approximation Techniques for Energy-Efficient Multipliers', in Proceedings of 56th ACM/IEEE Design Automation Conference (DAC), pp. 1-6.

[17] Wang J, S. Kuang, and S. Liang (2011), 'High-Accuracy Fixed-Width Modified Booth Multipliers for Lossy Applications', IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 19, no. 1, pp. 52-60.

[18] Y. Chen, and T. Chang (2020), 'A High-Accuracy Adaptive Conditional- Probability Estimator for Fixed-Width Booth Multipliers," IEEE Transactions on Circuits and Systems I (TCAS-I): Regular Papers, vol. 59, no. 3, pp. 594-603.

[19] S. Choi, G. Kim, H. Yoo, and B. Nam (2014), 'Hybrid radix-4/-8 truncated multiplier for mobile GPU applications', Electronics Letters, vol. 50, no. 23, pp. 1680-1682.

[20] W. Liu, L. Qian, C. Wang, H. Jiang, J. Han, and F. Lombardi (2017), 'Design of approximate radix-4 Booth multipliers for error-tolerant computing', IEEE Transactions on Computers, vol. 66, no. 8, pp. 1435-1441.

[21] V. Leon, G. Zervakis, D. Soudris, and K. Pekmestzi (2018), 'Approximate Hybrid High Radix Encoding for Energy-Efficient Inexact Multipliers', IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 26, no. 3, pp. 421-430.

[22] S. Venkatachalam, E. Adams, H. J. Lee and S. Ko (2019), 'Design and Analysis of Area and Power Efficient Approximate Booth Multipliers', IEEE Transactions on Computers, vol. 68, no. 11, pp. 1697-1703.

[23] Bipul Boro, K. Manikantta Reddy, Y.B. Nithin Kumar, M.H. Vasantha (2020), 'Approximate radix-8 Booth multiplier for low power and high-speed applications', Microelectronics Journal, vol. 101, pp. 1-14.

[24] J. Liang, J. Han and F. Lombardi (2013), 'New Metrics for the Reliability of Approximate and Probabilistic Adders', IEEE Transactions on Computers, vol. 62, no. 9, pp. 1760-1771.